**TABLE OF CONTENTS**

**Page**

**TITLE PAGE** i

**APPROVAL SHEET** ii

**ABSTRACT** iii

**DEDICATION** iv

**ACKNOWLEDGMENT** v

**TABLE OF CONTENTS** vi

**LIST OF FIGURES** xi

**LIST OF TABLES** xii

**CHAPTER 1: INTRODUCTION**  1

1.1 Background of the Study 1

1.2 Statement of the Problem 2

1.3 Objectives of the Study 3

1.4 Significance of the Study 3

1.5 Scope and Limitations 4

1.6 Definition of Terms 5

1.7 Theoretical Framework 9

1.7.1 Hardware 9

1.7.1.1 SoCKit Development Board 9

1.7.1.1.1 Cyclone V SoC 11

1.7.1.1.1.1 Dual-Core ARM Cortex-A9 13  
 MPCore Processor

1.7.1.1.2 USB 3300 Hi-Speed USB Host, 14  
 Device or OTG PHY

1.7.1.1.3 KSZ9021RL/RN Gigabit Ethernet 15  
 Transceiver

1.7.1.1.4 VGA 16

1.7.1.1.5 Memory 17

1.7.1.2 Logitech C525 Webcam 18

1.7.1.3 Micro SD Card 18

1.7.2 Software 19

1.7.2.1 In-System 19

1.7.2.1.1 Linux Kernel 19

1.7.2.1.2 Debian Operating System 19

1.7.2.1.3 OpenCV Library 20

1.7.2.1.4 Lightweight X11 Desktop 20  
 Environment (LXDE)

1.7.2.2 Development Software 21

1.7.2.2.1 Altera Quartus 21

1.7.2.2.2 Qsys - Altera’s System Integration Tool 21

1.7.2.2.3 SoC Embedded Design Suite 22

1.7.2.2.4 Linaro Toolchain 22

1.7.2.2.4.1 Linaro GCC 22

1.7.2.2.5 Github 23

1.7.2.2.6 Win32 Disk Imager 23

1.7.2.2.7 PuTTY 24

1.7.2.2.8 Others 24

**CHAPTER II: Review of Related Literature**  25

2.1 OpenCV 25

2.2.1 QpenCV Face Detection 25

2.2.1.1 Rapid Object Detection using a Boosted 27

Cascade of Simple Features

2.2.1.2 AdaBoost 28

2.2.1.3 FPGA-Based Face Detection System 28

Using Haar Classifiers

2.2.1.4 Object Detection Using the Statistics of Parts 29

2.2.1.5 A Parallel Architecture for Hardware 29

Face Detection

2.2.2 OpenCV Face Recognition 29

2.2 Current State of OpenCV Acceleration. 30

2.2.1 OpenCV GPU 31

2.2.2 OpenCV IPP 31

2.2.3 OpenCV Applications with Zynq-7000 All 32  
 Programmable SoC

2.3 USB Video Class 32

**CHAPTER III: Methodology** 34

3.1 System Requirements 34

3.2 Top Level Face Detection System Design Overview 35

3.3 Hardware Preparation 36

3.4 Development Environment Preparation 36

3.5 Integration Layer 37

3.5.1 Golden Hardware Reference Design 37

3.6 OS Layer 38

3.6.1 Modified Linux Kernel Source 38

3.6.2 U-Boot Configuration 39

3.6.3 SD Card Image 39

3.6.3.1 The Debian Based Linaro Ubuntu Image 39

3.6.3.2 Partitioning of the SD Card Image 39

3.6.3.3 System Files 40

3.6.4 Utilities 40

3.6.5 OpenCV Library 41

**CHAPTER IV: Result and Discussions** 42

4.1 System Integration 42

4.2 Linux System 43

4.3 OpenCV Library & Face Detection 44

4.4 Performance Comparison 45

4.5 System Bugs 46

4.5.1 USB UVC Bandwidth Issues with USB OTG 46

4.5.2 USB UVC has some issues FFMPEG 47

**CHAPTER V: Conclusion and Recommendation** 48

5.1 Conclusion 48

5.2 Recommendations 49

**REFERENCES** 50

**APPENDICES** 56

**Appendix A:** Expanded Block Diagram of the Face Detection System56

**Appendix B:** SoCKit Development Kits & Tools Detail57

**Appendix C:** ARM® Cortex™-A9 MPCore™ Specification59

**Appendix D:** FPGA Configuration Mode60

**Appendix E:** Configuring U-Boot63

**Appendix F:** From RocketBoards Org On How to Partition a uSD Card 64

**Appendix G:** Specs of the Intel CISC based system65

**Appendix H:** Kernel Panic Logs66

**Appendix I:** Researcher’s Notes on SoCKit Usage68

**Appendix J:** Face Detection System SoCKit Test Results72

**Appendix K:** Standard 512x512 pixels test image 73

**Appendix L:** Intel CISC Based Core i7 Test Results74

**Appendix M:** Source code used for performance comparison75

**CURRICULUM VITAE** 81

**LIST OF FIGURES**

**FIGURE PAGE**

Figure 1. System Block Diagram of the SoCKit Evaluation Board 10

Figure 2. Cyclone V SoC Integrated Circuit Block Diagram 12

Figure 3. Cortex A9 MPCore 13

Figure 4. Basic ULPI USB Device Block Diagram 14

Figure 5. Connections between Cyclone V SOC and FPGA and Ethernet 14

Figure 6. Functional Block Diagram of the KSZ9021RL/RN 16

Figure 7. VGA Block Diagram 17

Figure 8. Connections between FPGA and DDR3 18

Figure 9. Top Level block diagram of the Entire System. 34

Figure 10. Top Level System Overview 35

Figure 11. Development Tools 37

Figure 12. Boot Process 40

Figure 13. Hardware Design using Altera QSys 42

Figure 14. Successful compilation 43

Figure 15. Linux Build environment toolset 44

Figure 16. Menuconfig tool 45

Figure 17. Successfully compiled the face detection program 46

**LIST OF TABLES**

**TABLE PAGE**

Table 1 Comparrison of CISC based and Cyclon V SoC. 45